CLAIMS

What is claimed is:

1. A system comprising:

a core processing circuit; and

a host processing system coupled to the core processing system through a host bridge, the host processing system comprising:

logic to place the core processing circuit in a reset state; and

logic to load a reset vector to one or more registers at a boot address associated with the core processing circuit, the reset vector comprising one or more instructions to fetch addition instructions to initialize the core processing circuit upon release from the reset state.

2. The system of claim 1, wherein the registers are formed in one of a cache memory array associated with the core processing circuit and a memory coupled to the core processing circuit through a data bus.

3. The system of claim 1, wherein the host processing system comprises a system memory, and wherein the reset vector comprises at least one instruction to fetch data from a system memory coupled to the core processing circuit through the host bridge.

4. The system of claim 3, wherein the host processing system further comprises logic to set an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit.

5. The system of claim 3, wherein the host processing system further comprises logic to initiate one or more write bus transactions at an address translation unit to load the reset vector in the registers while the core processing circuit is in the reset state, and wherein the core processing circuit comprises logic to initiate one or more read bus transactions at the address translation unit addressed to the system memory in response to execution of the interrupt vector upon release from the reset state.

6. The system of claim 1, wherein the host processing system further comprises logic to release the core processing circuit from the reset state in response to loading the reset vector at the boot address.

7. The system of claim1, wherein the additional instructions comprise instructions to commence a power-on self test procedure.

8. The system of claim 7, wherein the additional instructions further comprise instructions to launch an operating system to the core processing circuit.

9. A method comprising:

placing a core processing circuit in a reset state; and

loading a reset vector to one or more registers at a boot address associated with the core processing circuit, the reset vector comprising one or more instructions to fetch additional instructions from a system memory coupled to the core processing circuit through a host bridge of a host processing system.

10. The method of claim 9, the method further comprising loading the reset vector to a boot address in registers formed in one of a cache memory associated with the core processing circuit and a memory coupled to the core processing circuit through a data bus.

11. The method of claim 9, wherein the method further comprises setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit.

12. The method of claim 9, wherein the method further comprises:

initiating one or more write bus transactions at an address translation unit to load the reset in the registers while the core processing circuit is in the reset state; and

initiating one or more read bus transactions at the address translation unit addressed to the system memory in response to execution of the interrupt vector upon release of the core processing circuit from the reset state.

13. The method of claim 9, wherein the additional instructions further comprise instructions to commence a power-on self test procedure.

14. The method of claim 13, wherein the additional instructions further comprise instructions to launch an operating system to the core processing circuit.

15. A method comprising:

placing a core processing circuit in a reset state; and

loading instructions from a system memory of a host processing system to one or more registers at a boot address associated with the core processing circuit, the instructions comprising one or more instructions to initialize the core processing circuit upon release of the core processing circuit from the reset state.

16. The method claim 15, wherein the method further comprises transmitting the instructions from the system memory through a host bridge of the host processing system.

17. The method of claim 15, the method further comprising releasing the core processing circuit from the reset state in response to loading the instructions at the boot address.

18. The method of claim 15, the method further comprising loading the instructions to a boot address in registers formed in one of a cache memory associated with the core processing circuit and a memory coupled to the core processing circuit through a data bus.

19. The method of claim 15, wherein the method further comprises setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit.

20. The method of claim 15, wherein the instructions comprise instructions to commence a power-on self test procedure.

21. The method of claim 20, wherein the instructions further comprise instructions to launch an operating system to the core processing circuit.

22. An article comprising:

a storage medium comprising machine-readable instructions encoded there on for:

placing a core processing circuit in a reset state; and

loading a reset vector to one or more registers at a boot address associated with the core processing circuit, the reset vector comprising one or more instructions to fetch additional instructions from a system memory coupled to the core processing circuit through a host bridge of a host processing system.

23. The article of claim 22, wherein the storage medium further comprising machine readable instructions stored thereon for loading the reset vector to a boot address in registers formed in one of a cache memory associated with the core processing circuit and a memory coupled to the core processing circuit through a data bus.

24. The article of claim 22, wherein the storage medium further comprises machine readable instructions stored thereon for setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit.

25. The article of claim 22, wherein the storage medium further comprises machine readable instructions stored thereon for initiating one or more write bus transactions at an address translation unit to load the reset vector in the registers while the core processing circuit is in the reset state.

26. The article of claim 22, wherein the storage medium further comprises machine readable instructions stored thereon for releasing the core processing circuit from the reset state in response to loading the reset vector at the boot address.

27. The article of claim 22, wherein the additional instructions comprise instructions to commence a power-on self test procedure.

28. The article of claim 27, wherein the additional instructions further comprise instructions to launch an operating system to the core processing circuit.

29. An article comprising:

a storage medium comprising machine-readable instructions encoded there on for:

placing a core processing circuit in a reset state; and

loading instructions from a system memory of a host processing system to one or more registers at a boot address associated with the core processing circuit, the instructions comprising one or more instructions to initialize the core processing circuit upon release from the reset state.

30. The article of claim 29, wherein the storage medium further comprises machine readable instructions stored thereon for transmitting the instructions from the system memory through a host bridge of the host processing system.

31. The article of claim 29, wherein the storage medium further comprising machine readable instructions stored thereon for releasing the core processing circuit from the reset state in response to loading the instructions at the boot address.

32. The article of claim 29, wherein the storage medium further comprises machine readable instructions stored thereon for loading the instructions to a boot address in registers formed in one of a cache memory associated with the core processing circuit and a memory coupled to the core processing circuit through a data bus.

33. The article of claim 29, wherein the storage medium further comprises machine readable instructions stored thereon for setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit.

34. The article of claim 29, wherein the instructions comprise instructions to commence a power-on self test procedure.

35. The article of claim 34, wherein the instructions further comprise instructions to launch an operating system to the core processing circuit.